CLAIMS

What is claimed is:

1. A method of forming silicon wires in a single crystal silicon substrate, the method comprising:

defining lines having a width;

creating columns corresponding to the lines, the columns having ripples on both sides with a width comparable to the width of the lines; and

oxidizing the columns to create silicon wires substantially corresponding to the ripples.

2. The method of claim 1 wherein the width of the ripples is approximately equal to one-half the width of the lines.

3. The method of claim 1 wherein the ripples are created by cyclically etching and passivating the columns.

4. The method of claim 3 wherein the cycle time is between approximately 6 and 30 seconds.

5. The method of claim 3 wherein etching comprises isotropic reactive ion etching.

6. The method of claim 5 wherein SF_6 is used in the deep reactive ion etch.

7. The method of claim 1 wherein the ripples are formed by a Bosch process.

8. A method of forming nano-structures in a semiconductor substrate, the method comprising:

defining columns in the substrate;

repetitively etching and passivating sides of the column to create a column having ripples; and

oxidizing the ripples to form nano-structures.

9. A method of creating a three dimensional array of wires in silicon substrate, the method comprising:

defining an array of intersecting lines;

creating columns corresponding to the lines, the columns having ripples on both sides with a width comparable to the width of the lines; and

forming silicon wires substantially corresponding to the ripples, and extending between the columns defined by the support lines.

10. The method of claim 9 wherein the width of lines and gap between lines is periodic in three dimensions for creating a photonic bandgap structure.

11. The method of claim 9 wherein forming silicon wires comprises oxidizing, or aggressively etching the columns.

12. A method of creating a three dimensional array of wires in silicon substrate, the method comprising:

defining support pillars on the substrate, the pillars having a first width;

defining wire lines on the substrate extending between the support pillars, and having a second width narrower than the first width;

creating sidewalls corresponding to the support pillars and wire lines, the sidewalls having ripples on both sides with a width comparable to the width of the wire lines; and

forming silicon wires substantially corresponding to the ripples, and extending between the pillars.

13. The method of claim 12 wherein forming silicon wires comprises oxidizing, or aggressively etching the columns.

14. A method of forming wires in a semiconductor substrate, the method comprising:

defining a column;

repetitively etching and polymerizing sides of the column to create a column having ripples; and

oxidizing the column to form a wire surrounded by oxide.

15. A method of forming wires in a semiconductor substrate, the method comprising:

defining a column by use of a mask, wherein areas of the substrate adjacent the column comprise a floor;

repetitively etching the floor to create a column having rough sides;

passivating the etched column and floor between each etch;

clearing the floor of the substrate before each etch; and

oxidizing the column to form a wire surrounded by oxide.

16. A pair of columns formed from a semiconductor substrate, the columns comprising:

multiple wires of silicon extending parallel to a floor of the substrate between the pair of columns; and

oxide surrounding each wire.

17. A method of creating a three dimensional array of nano-tips in a silicon substrate, the method comprising:

defining support lines on the substrate having a first width;

defining wire lines on the substrate extending between the support lines, and having a second width narrower than the first width;

creating columns corresponding to the support lines and wire lines, the columns having ripples on both sides with a width comparable to one-half the width of the wire lines; and

oxidizing the columns to create silicon tips substantially corresponding to the ripples, and extending partially between the columns defined by the support lines.

18. The method of claim 17 and further comprising removing oxide to expose the silicon nano-tips.

19. A method of forming channels in a semiconductor substrate, the method comprising:

defining a trench having two sides;

repetitively etching and passivating the sides of the trench to create rough sides; and

oxidizing the trench to form a channel surrounded by oxide.

20. A method of forming channels in a semiconductor substrate, the method comprising:

defining two side walls by use of a mask, wherein areas of the substrate adjacent the side walls comprise a floor;

repetitively etching the floor to create side walls having rough sides;

polymerizing the etched sidewalls and floor between each etch;

clearing the floor of the substrate before each etch; and

oxidizing the side walls to form a channel between the sidewalls corresponding to at least one of the etches.

21. A method of forming a sieve from a semiconductor substrate, the method comprising:

defining multiple columns in the substrate;

repetitively etching and passivating the columns to form ripples on the columns;

etching the rippled columns to form wires substantially corresponding to the ripples; and

oxidizing the wires to reduce spacing between the wires.

22. The method of claim 21 wherein the columns are defined with a decreasing line spacing, resulting in a progressively reduced spacing between the wires.

23. A three dimensional lattice of wires formed from a semiconductor substrate comprising:

an array of parallel pillars; and

multiple micron to sub micron diameter silicon wires extending between the pillars.

24. The three dimensional lattice of wires of claim 23, wherein the pillars comprise pillars internal to the array, and pillars defining an outside edge of the array, wherein the internal pillars have multiple sets of wires extending perpendicular from each pillar toward another pillar.

25. The three dimensional lattice of wires of claim 24 wherein each set of wires comprises three substantially parallel silicon wires.

26. The three dimensional lattice of wires of claim 23 wherein each wire is oxidized to create a sieve of desired wire spacing.

27. The three dimensional lattice of wires of claim 26 wherein pillar spacing is progressively smaller to create a graded sieve.

28. The three dimensional lattice of wires of claim 23 wherein the pillar and wire spacing is selected to form a photonic bandgap structure

29. The three dimensional lattice of wires of claim 23 wherein the wires are periodic with respect to each other.

30. The three dimensional lattice of wires of claim 23 wherein the wires form hexagonal shapes.

31. A method of creating a displacement sensor supported by a substrate, the method comprising:

defining a column by use of a mask, the column comprising thicker support structures on both ends, wherein areas of the substrate adjacent the column comprise a floor;

repetitively etching the floor to create a column having rough sides;

passivating the etched column and floor between each etch;

clearing the floor of the substrate before each etch; and

oxidizing the column to form a wire surrounded by oxide which is thicker on both ends, and fully oxidized in the middle to form opposed tips a desired distance apart and supported by the support structures.

32. The method of claim 31 wherein the distance is controlled to ensure that tunneling current via quantum effect is modified by slight displacements of the support structures.

33. A displacement sensor comprising:

a pair of opposing support structures;

a wire extending between the support structures, wherein the wire is oxidized such that it is thicker at the support structures and fully oxidized between the support structures such that the wire forms opposed tips a desired distance apart.

34. A three dimensional lattice of wires formed from a semiconductor substrate comprising:

an array of parallel pillars;

rows of multiple micron to sub micron diameter silicon wires extending between the pillars forming hexagonal shapes supported by the pillars; and

a waveguide disposed between two of such rows.

35. The three dimensional lattice of wires of claim 34, wherein the pillars support multiple layers of wires forming layers of hexagonal shapes.

36. A three dimensional lattice of tips formed from a semiconductor substrate comprising:

an array of parallel pillars; and

a nanotip on each pillar extending substantially perpendicular from the pillar to an adjacent pillar.

37. The three dimensional lattice of tips of claim 36 wherein tips on adjacent pillars point toward each other.

38. The three dimensional lattice of tips of claim 36 wherein each pillar has multiple tips dispersed along it's height.

39. The three dimensional lattice of tips of claim 36 wherein the tips comprise silicon.